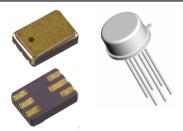


NPN Dual Silicon Transistors

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Features

- Available in JAN, JANTX, JANTXV, JANS and JANSR per MIL-PRF-19500/495
- TO-78 and U package types
- · Radiation Tolerant Levels M, D, P, L, and R



Electrical Characteristics (T_A = +25°C unless otherwise specified)

Parameter	Test Conditions	Symbol	Units	Min.	Max.		
Off Characteristics							
Collector - Emitter Breakdown Voltage	I _C = 10 mA dc	V _{(BR)CEO}	V dc	40	_		
Collector - Base Cutoff Current	V_{CB} = 75 V dc V_{CB} = 50 V dc	I _{CBO1}	μA dc nA dc	_	10 10		
Emitter - Base Cutoff Current	V_{EB} = 6.0 V dc V_{EB} = 4.0 V dc	I _{EBO1}	μΑ dc nA dc	_	10 10		
On Characteristics ¹			· · · · · · · · · · · · · · · · · · ·				
Forward Current Transfer Ratio	$ 2N5793, A \\ V_{CE} = 10 V dc; I_C = 0.1 mA dc \\ V_{CE} = 10 V dc; I_C = 1.0 mA dc \\ V_{CE} = 10 V dc; I_C = 10 mA dc \\ V_{CE} = 10 V dc; I_C = 150 mA dc \\ V_{CE} = 10 V dc; I_C = 300 mA dc \\ V_{CE} = 1.0 V dc; I_C = 150 mA dc \\ V_{CE} = 1.0 V dc; I_C = 1.0 mA dc \\ V_{CE} = 10 V dc; I_C = 0.1 mA dc \\ V_{CE} = 10 V dc; I_C = 1.0 mA dc \\ V_{CE} = 10 V dc; I_C = 150 mA dc \\ V_{CE} = 10 V dc; I_C = 300 mA dc \\ V_{CE} = 10 V dc; I_C = 300 mA dc \\ V_{CE} = 1.0 V dc; I_C = 150 mA dc \\ V_{CE} = 1.0 V $	h _{FE1} h _{FE2} h _{FE3} h _{FE4} h _{FE5} h _{FE6}	h _{FE}	20 25 35 40 25 20 35 50 75 100 40 50	120 300		
Collector - Emitter Saturation Voltage	I_{C} = 150 mA dc, I_{B} = 15 mA dc I_{C} = 300 mA dc, I_{B} = 30 mA dc	V _{CE(SAT)1}	Vdc	_	0.3 0.9		
Base - Emitter Saturation Voltage	I_C = 150 mA dc, I_B = 15 mA dc	V _{BE(SAT)1}	Vdc	0.6	1.2		
Base - Emitter Saturation Voltage	I_C = 300 mA dc, I_B = 30 mA dc	V _{BE(SAT)2}	Vdc	_	1.8		
Forward-Current Transfer Ratio (Gain Ratio) (2N5793A, 2N5794A, 2N5794AU)	V_{CE} = 10 V dc; I_C = 1 mA dc	h _{FE2-1} —— h _{FE2-2}		0.9	1.11		

^{1.} Pulse Test: Pulse Width = 300 µs, Duty Cycle ≤2.0%.



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Electrical Characteristics (T_A = +25°C unless otherwise specified)

Parameter	Test Conditions	Symbol	Units	Min.	Max.	
Forward-Current Transfer Ratio (Gain Ratio) (2N5793A, 2N5794A, 2N5794AU)	V_{CE} = 10 V dc; I_{C} = 10 mA dc	h _{FE3-1} —— h _{FE3-2}		0.9	1.11	
Absolute Value of Base Emitter-Voltage Differential (2N5793A, 2N5794A, 2N5794AU)	V_{CE} = 10 V dc; I_C = 1 mA dc	V _{BE1-} V _{BE2}	mV dc	_	10	
Collector-Base Cutoff Current	T _A = +150°C V _{CB} = 50 V dc	I _{CBO3}	μA dc	_	10	
Forward Current Transfer Ratio	$T_A = -55^{\circ}\text{C}$ $V_{CE} = 10 \text{ V dc}; I_C = 150 \text{ mA dc}$ $2N5793, 2N5793A$ $2N5794, 2N5794U$ $2N5794A, 2N5794AU$	h _{FE7}		16 40 40		
Dynamic Characteristics						
Magnitude of Common Small-Signal Short-Circuit Forward Current Transfer Ratio	I _C = 20 mA dc; V _{CE} = 20 V dc; f = 100 MHz	h _{FE}	-	2.0	10	
Open Circuit Output Capacitance	$V_{CB} = 10 \text{ V dc}; I_{E} = 0 \text{ mA}; 100 \text{ kHz} \le f \le 1 \text{ MHz}$	C_{obo}	pF	_	8.0	
Input Capacitance (Output Open- Circuited)	$V_{EB} = 0.5 \text{ V dc}; I_C = 0; 100 \text{ kHz} \le f \le 1 \text{ MHz}$	C _{ibo}	pF	_	33	
Switching Characteristics						
Turn-On Time (saturated)	V_{CC} = 30 V dc; I_C = 150 mA dc; I_{B1} = 15 mA dc; $V_{BE(OFF)}$ = 0.5 V dc	t _{on}	ns	_	45	
Turn-Off Time (saturated)	V_{CC} = 30 Vdc; I_C = 150 mA dc; I_{B1} = I_{B2} = 15 mA dc	t _{off}	ns	_	310	



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Absolute Maximum Ratings (T_A = +25°C unless otherwise specified)

Ratings	Symbol	Value
Collector - Emitter Voltage	V _{CEO}	40 V dc
Collector - Base Voltage	V _{CBO}	75 V dc
Emitter - Base Voltage	V _{EBO}	6.0 V dc
Collector Current	I _C	600 mA dc
Total Power Dissipation @ T _A = +25°C One Section Both Sections	P _T (1)	500 mW 600 mW
Operating & Storage Temperature Range	T _J , T _{STG}	-65°C to +175°C

Thermal Characteristics							
Types	R _{•JA} One Section	R _{•JA} Both Sections	R _{∘JSP} One Section	R _{∘JSP} Both Sections	R _{∘JPCB} One Section	R _{∗JPCB} Both Sections	
2N5793, 2N5794 2N5793A, 2N5794A	°C/W ⁽²⁾ 350 350	°C/W ⁽²⁾ 290 290	°C/W ⁽²⁾	°C/W ⁽²⁾	°C/W (2)	°C/W ⁽²⁾	
2N5794U, 2N5794AU			110 110	90 90	350 350	290 290	

⁽¹⁾ For $T_A > +25^{\circ}C$, derate linearly 2.86 mW/°C one section, 3.43 mW/°C both sections

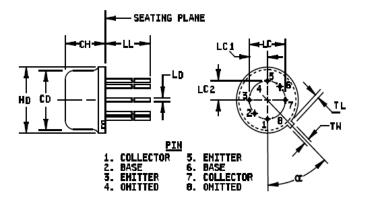
⁽²⁾ For the thermal resistance curves see figures 4, 5 and 6 of MIL-PRF-19500/495



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Outline Drawing



Dimensions						
O mala al	Inches		Millin	Note		
Symbol	Min	Max	Min	Max	Note	
CD	.305	.335	7.75	8.51		
CH	.150	.185	3.81	4.70		
HD	.335	.370	8.51	9.40		
LD	.016	.021	0.41	0.53		
LL	.500		12.70			
LC	.200 BSC		5.08	BSC	4	
LC1	.100 BSC		2.54 BSC			
LC2	.100 BSC		2.54 BSC			
TL	.029	.045	0.74	1.14	3	
TW	.028	.034	0.71	0.86		
α	45° TP		45	, Lb	6	

NOTES:

- Dimensions are in inches.
- 2. Millimeters are given for general information only.
- 3. Measured from maximum diameter of the product.
- Leads having maximum diameter .019 inch (.483 mm) measured in gaging plan .054 inch (1.37 mm) + .001 inch (.025 mm) .000 inch (.000 mm) below the seating plane of the product shall be within .007 inch (.178 mm) of their true position relative to a maximum width tab.
- The product may be measured by direct methods or by gauge.
- Tab centerline.
- In accordance with ASME Y14.5M, diameters are equivalent to \(\phi x \) symbology.

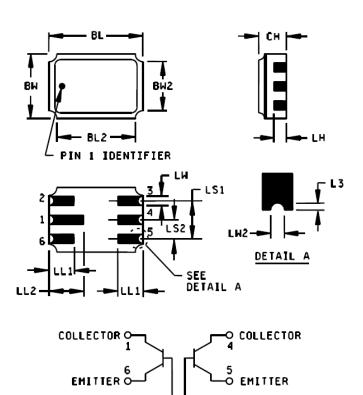
FIGURE 1. Physical dimensions (2N5793 and 2N5794) (similiar to TO-99).



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Outline Drawing



		Dime	ensions			
Symbol	In			Millimeters		
Symbol	Inches					
	Min	Max	Min	Max		
BL	.240	.250	6.10	6.35		
BL ₂		.250		6.35		
BW	.165	.175	4.19	4.45		
BW ₂		.175		4.45		
CH	.058	.100	1.47	2.54		
L ₃	.003	.007	0.08	0.18		
LH	.026	.039	0.66	0.99		

	Dimensions				
Symbol	Inches		Millimeters		
	Min	Max	Min	Max	
LL ₁	.060	.070	1.52	1.78	
LL ₂	.082	.098	2.08	2.49	
LS ₁	.095	.105	2.41	2.67	
LS ₂	.045	.055	1.14	1.40	
LW	.022	.028	0.56	0.71	
LW ₂	.006	.022	0.15	0.56	

NOTES:

- Dimensions are in inches.
- 2. Millimeters are given for general information only.
- Dimension "CH" controls the overall package thickness.
- The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option from that shown on the drawing.
- 5. Dimensions "LW2" minimum and "L3" minimum and the appropriate castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on bottom two layers, optional on top ceramic layer.) Dimension "LW2" maximum and "L3" maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.
- Lead 4 = collector.
- 7. In accordance with ASME Y14.5M, diameters are equivalent to φx symbology

FIGURE 2. Physical dimensions, 2N5794U.



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Maximum Thermal Impedance

023F Half-Dual Chip LCC6 (U) Theta-JSP (Infinite Mount) Tsp=25C

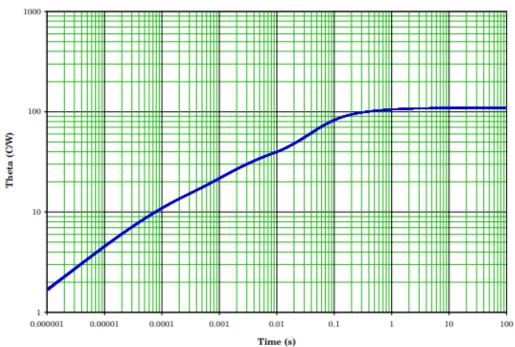


FIGURE 4. Thermal impedance graph (R_{BJSP}) for 2N5794U, 2N5794UC, 2N5794AU, and 2N5794AUC (U and UC).



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Maximum Thermal Impedance

023F Dual Chip LCC6 (U) Theta-JA (FR4 PCB Mount) Ta=25C

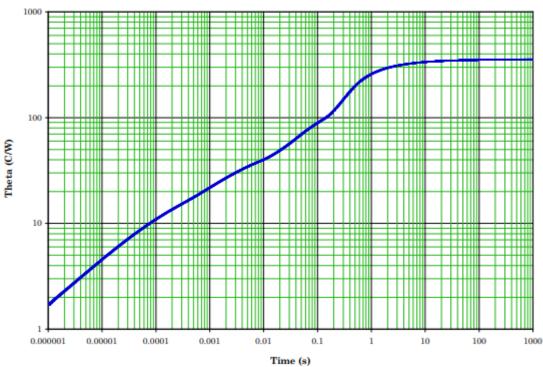


FIGURE 5. Thermal impedance graph (R_{BJPCB}) for 2N5794U, 2N5794UC, 2N5794AU, and 2N5794AUC (U and UC).



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Maximum Thermal Impedance

TO-78 with 023F Chip Thermal Impedance per Side with Other Side Equally Biased

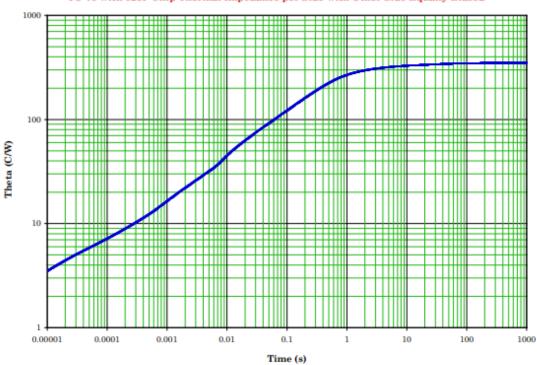


FIGURE 6. Thermal impedance graph (R_{0,JA}) for 2N5794U, 2N5794UC, 2N5794AU, and 2N5794AUC (U and UC).



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